

[DRAM CIRCUITRY WITH A LONGER REFRESH PERIOD]

Abstract of Disclosure

A DRAM circuitry includes a DRAM cell that is connected at a first end to a bit line, at a second end to a plate line, and at a third end to a word line, and a sensing amplifier that is electrically connected to the DRAM cell for refreshing the DRAM cell and reading data from the DRAM cell. The sensing amplifier can change a potential of the bit line and a potential of the plate line to write data into the DRAM cell when the word line is turned on.

09:22:44.080704
"FOCUS" 4228960

Figures

096324-030301
T020304-030301